

APPLICATION
FOR
UNITED STATES LETTERS PATENT

TITLE: DESIGNS AND METHODS FOR CONDUCTIVE BUMPS
APPLICANT: VALERY M. DUBIN, SRIDHAR BALAKRISHNAN AND
MARK BOHR

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EV348187427US

September 22, 2003
Date of Deposit

Designs and Methods for Conductive Bumps

TECHNICAL FIELD

This specification relates to semiconductor process fabrication, and more particularly to fabricating bumps for integrated circuits, as in die packaging.

BACKGROUND

5 During a die packaging process, several conductive layers may be placed between the substrate of a die and the surrounding package. The die package can be soldered with a conductive layer and the soldered layer may contact a lower-level conducting layer. The lower-level conducting layer may be patterned to have one or more conducting bumps, and may be referred to as a “bump” layer. A bump may contact a base layer metal (BLM) that is directly or
10 indirectly connected to the substrate. The bump and the base layer metal may have one or more properties that may result in one or more electromigration issues or degradation of the layers.

DESCRIPTION OF DRAWINGS

FIGS. 1A-1D show exemplary defective bump diagrams.

FIG. 2 shows an exemplary implementation of the fabricated structure.

15 FIG. 3 is an exemplary flow diagram of the fabrication of the exemplary implementation shown in FIG. 2.

FIG. 4 shows an exemplary implementation of the fabricated structure.

FIG. 5 is an exemplary flow diagram of the fabrication of the exemplary implementation shown in FIG. 4.

20 FIG. 6 shows an exemplary implementation of the fabricated structure.

FIG. 7 is an exemplary flow diagram of the fabrication of the exemplary implementation shown in FIG. 6.

FIG. 8 shows an exemplary implementation of the die package structure in an electrical/computer system.

DETAILED DESCRIPTION

The techniques, methods, and structures of one or more exemplary implementations in the present disclosure relate to integrated circuits and die packaging. In particular, one or more

exemplary implementations relate to fabricating bumps on a substrate to prevent Cu and Sn intermixing. One or more exemplary implementations in the present disclosure may reduce a number of electromigration issues relating to CuSn intermetallic formation, and may reduce the formation of whiskers in one or more layers.

5 The details of one or more exemplary implementations are set forth in the accompanying drawings and the description below. In one exemplary implementation, an apparatus comprises a semiconductor substrate and a first conducting layer in contact with the semiconductor substrate. The first conducting layer may comprise a base layer metal, such as Cu. The apparatus further comprises a diffusion barrier in contact with the first conducting layer, a wetting layer on top of
10 the diffusion barrier, and a bump layer on top of the wetting layer. The bump layer may include Sn, and the Sn bump layer may be electroplated. The diffusion barrier may prevent Cu and Sn from diffusing through the diffusion barrier. The diffusion barrier may also be able to suppress a whisker-type formation in the bump layer. Other features and advantages of one or more exemplary implementations will be apparent from the description and drawings, and from the
15 claims.

 In semiconductor wafer processing, devices and interconnects are formed on a substrate and are electrically connected to a die package. An electrical connection to a die package may be achieved with a conducting solder layer between the die package and a lower-level conducting interconnect layer on the wafer. The solder layer may oftentimes include Sn or a Sn alloy. The
20 conducting interconnect layer, or an adjacent conducting layer, may oftentimes include Cu. In some cases, the conducting interconnect layer may be the lowest level metal layer or the metal layer that is in closest proximity to the substrate. Such a metal layer may be referred to as a base layer metal (BLM). In some cases, the base layer metal may be used as a diffusion barrier to prevent solder from migrating into a lower-level pad of the die. The pad of the die may include
25 one or more layers of metal, such as an Al layer. In one or more exemplary implementations of the present disclosure, a layer may be formed on top of the base layer metal to serve as a diffusion barrier between Cu in the base layer metal and Sn in a layer above the diffusion barrier.

 A die package interconnect structure with Sn in one layer and Cu in a nearby layer may result in one or more detrimental issues for the die package interconnect. Some of these
30 detrimental issues may degrade the electrical and mechanical properties of the die package interconnect, reduce the yield of forming such interconnects, or even form irregular, unintended

regions such as whiskers and delaminations. Delamination may involve the degradation or the physical separation of one or more layers. Some of these detrimental issues are exemplified in Figs. 1A-1D and are described below.

Figs. 1A-1B present diagrams of a die package interconnect with an exemplary bump delamination. The bump 110 in the diagram of Fig. 1A is a solder region that includes a Sn alloy, PbSn. As shown in a marked region 115, a bump 110 may conform to the shape of the lower interconnect or the base layer metal 125. The bump 110 may contact and cover the edges and sidewalls of lower interconnects or the base layer metal.

Fig. 1B is a diagram of the region 115 in which the base layer metal 125, the PbSn bump 110, and the die substrate area 130 are presented. In this diagram, delamination occurs in the layers 125, 110 between the substrate 130 and the bump 110. Such delamination may result from one or more properties of the base layer metal 125. The base layer metal 125 may be constructed in such a manner that the base layer metal 125 may degrade during baking or thermal processing. Degradation and delamination may reduce the conducting surface area between the layers 125, 110 and create electromigration-related failures.

Some failures in die package interconnects may be electromigration-related failures and other failures may be due to the properties of the layer materials and the interfacing of layers. Some electromigration-related failures may be due to the metallurgical properties of the layers 125, 110, increased heat and thermal issues, and the growth of one or more voids 120 between the layers 125, 110. Electromigration in region 115 may create higher current densities and increase electromagnetic stress. As described below in one or more exemplary implementations, methods, structures, and techniques are presented to reduce electromigration-related die package interconnect failures.

Certain metallurgical properties of one or more layers of die package interconnects may result in die package interconnect failure. Examples of such metallurgical properties include non-conforming surfaces, phase transitions of materials at different temperatures, and diffusion and intermixing of elements of different layers. For instance, Sn can be a common metal used in one or more die package interconnect layers. However, Sn may exist in two allotropes at different temperatures. Above a temperature of about 13.2 °C, the hard, shiny, and conductive alpha Sn (tetragonal structure, α -phase Sn) may be in a stable phase. When the temperature is below 13.2 °C, beta Sn (diamond cubic structure, β -phase Sn) may be thermodynamically

favorable. The alpha phase is a preferred phase in a layer structure. The alpha to beta phase transformation may be accompanied by a 26% volume increase due to different densities of two phases. The change in volume in the phase transition may deform the interface between Sn and other layers. Also, beta Sn is in powder form and does not have the mechanical strength for an interconnect. Hence, when the Sn is in beta phase, the mechanical strength of the Sn layer and the interconnect deteriorates. For at least the above reasons, a Sn layer or interconnect can transition from alpha phase to beta phase during low temperatures and may lead to interconnect failure. As described below in one or more exemplary implementations, methods, techniques, and structures are presented to prevent low temperature phase transition of Sn.

Although bump 110 is shown as a solder bump in 100, the bump may be a bump or a bump layer that is not a solder layer, but a layer adjoining a solder layer. Moreover, the bump 110 may not be directly contacting the die package 105. As described in the figures below, the bump or bump layer could include other materials, such as Cu, and may contact directly to the base layer metal or other layer interconnects.

Figs. 1C-1D present examples of the undesirable intermixing of Cu and Sn of different layers. For instance, Fig. 1C shows a diagram of a die package interconnect 150 with a void 155 in a solder layer. Diffusion or intermixing of Cu and Sn from different layers may form CuSn intermetallics and may help to create the void 155. The electrical resistance in the interconnect 150 may increase due to voiding in the solder and may result in electromigration problems.

Other undesirable formations, such as whiskers, may also form due to the intermixing of Cu and Sn. The whiskers may result in compressive stress build up in Sn bumps and may lead to die package interconnect failure.

Fig. 1D shows another exemplary diagram 160 of various layers of a die package interconnect with diffused or intermixed Cu and Sn. Fig. 1D shows examples of Cu and Sn formation. For instance, a region 165 of Cu_3Sn and a region 170 of Cu_6Sn_5 have formed between layers of Cu 172, 178 and Sn 176 in the diagram 160.

Some conventional techniques attempt to prevent the intermixing and diffusion of Cu and Sn from different die package interconnect layers. For instance, the use of Pb5Sn bumps may be used to prevent whisker formation. However, the use of Pb5Sn bumps may have electromigration issues that may result from low temperature phase transition of Sn, as described above. Moreover, Pb may contribute to environmental and health issues. In another

conventional example, sputtered Ni may be used to prevent Cu diffusing into Sn. However, sputtered Ni has poor diffusion barrier properties and does not adequately prevent Cu and Sn diffusion or intermixing. As described below in one or more exemplary implementations, methods, techniques, and structures are presented to prevent the diffusion and intermixing of Cu and Sn between different die package interconnect layers.

One or more exemplary implementations in the present disclosure also present methods, techniques, and structures to prevent degradation of Sn bumps during etching of the base layer metal. In general, the corrosion and oxidation of the Sn bumps may be prevented during etching of a base layer metal that includes Ti, Al, or NiV.

Fig. 2 shows an exemplary implementation of a die package interconnect. A base layer metal 230 is formed on top of a silicon substrate 205 and the base layer metal 230 may include Cu. The base layer metal 230 may also be formed on top of a patterned insulator, resin, or dielectric layer 235, such as a polyimide layer. The base layer metal 230 may include an adhesion layer 232 and a seed layer 234. The adhesion layer 232 may be formed, for example, on the substrate 205 or a dielectric layer 235. The adhesion layer 232 may help in the joining or attaching of two different surfaces, such as helping the base layer metal to stick to the underlying surface. The seed layer 234 may help to build up the base layer metal structure on top of the adhesion layer 232. The seed layer may serve as a smooth interface to an underlying layer and may facilitate correct growth and formation of the base layer metal. The adhesion layer 232 may include Ti, TiN, and TiSiN and the seed layer 234 may include Ni, NiV, and Co. An additional metal layer, such as an Al layer 233, may be formed between the adhesion layer 232 and the seed layer 234 in order to improve one or more properties of the base layer metal. The improvement of the base layer metal properties with the additional metal layer may include the suppression of whisker formations and the prevention of layer delamination and degradations during thermal processing and electromagnetic stress.

A diffusion barrier layer 225 can be selectively positioned on top of the base layer metal 230. Selective deposition may mean that some surfaces may have another layer deposited only on a portion of that surface. The electroless diffusion barrier can prevent Cu and Sn from diffusing through the diffusion barrier. The diffusion barrier layer 225 may be electroless and located in a position to prevent the intermixing of Cu from the base layer metal 230 and Sn from the bump layer 215 or solder layer 210. The diffusion barrier layer 225 may prevent CuSn

intermetallic formation and whisker formation. The diffusion barrier layer 225 may prevent bump delamination and improve the processing yield of fabricating die package interconnects. The diffusion barrier layer 225 may include, among others, any one of CoBP, CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP.

5 Electroless deposits may offer one or more advantages when deposited on irregularly shaped objects, patterns, and recesses. In electroless plating, electrons are supplied by a chemical reducing agent. In general, electroless plating may refer to a reduction of metal ions from a solution containing a reducing agent. The reducing agent can supply electrons by oxidation on a catalytic surface. Electroless deposits may have high uniformity and little to no compressive stress during plating. Electroless deposits tend to be uniform in thickness over all of the shape of the underlying structure, therefore providing more uniform current densities and reducing some electromigration issues. Electroless barriers may also offer the advantages of being low cost, selective, and amorphous.

15 The diffusion barrier may have other materials that may prevent or inhibit the diffusion of Sn with Cu through the diffusion barrier. For example, platable materials having slow reaction or diffusion with Sn and Cu may be used, such as metals from group VIII (e.g., Co, Ni, Fe, Ru, Rh, Ir, and Os) alloying with Group VI (e.g., W, Mo, and Cr) and metalloid (e.g., B, P, and N).

A wetting layer (not shown) may be placed on top to the diffusion barrier layer 225. The wetting layer may also be selectively deposited on portions of the diffusion barrier layer 225. 20 The wetting layer may include any one of CoB, NiB, and NiP.

A bump layer 215 is placed on top of the wetting layer and a solder layer 210 is placed on top of the bump layer 215. The die package 220 is on top of and electrically connected to the solder layer 210. Electrical connection to the die package 220 may allow current to flow between the die package and devices and interconnects near or on the substrate. Sn may be in 25 the bump layer 215, the solder layer 210, or in both layers 210, 215.

In one or more exemplary implementations in the present disclosure, Sn may be electroplated to suppress whisker formation and related electromigration failures. The electroplating of Sn may also prevent low temperature (e.g., around 13.2 °C) phase transition of Sn and prevent mechanical and electromigration failures related to beta Sn. The electroplating of 30 Sn may include Sn and the alloys of Sn, such as 0.7Cu, Bi, Sb, and 3.5Ag. Sn may be electroplated at a constant current (e.g., around 10 - 100 mA/cm²) or voltage from a solution

containing Sn salt (e.g., Sn sulfate, Sn chloride), acid (e.g., sulfuric acid, sulfonic acid), and other additives (e.g., a suppressor, such as polyether glycol or grain refiner and an anti-oxidant).

Fig. 3 is an exemplary flow diagram of the fabrication of the exemplary implementation shown in Fig. 2. One or more devices and Cu interconnects may be formed on the wafer at 310. The die package interconnect 200 may then be passivated with SiN and polyimide at 312. By using lithography and etching operations, a contact pad (not shown) may be opened for Cu metallization. The base layer metal 230 may be deposited using plasma vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), or plating at 314. The base layer metal 230 may include an adhesion layer (e.g., Ti, TiN, or TiSiN) and a seed layer (e.g., Ni, NiV, or Co). An additional metal layer, such as Al, can be formed between the adhesion layer and the seed layer to improve barrier properties of the base layer metal 230.

A photoresist layer may then be deposited and patterned at 316. A diffusion barrier layer 225 can be formed at 318. The diffusion barrier layer 225 may be electroless and may include any one of CoBP, CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP. Then, a wetting layer can be deposited on the diffusion barrier layer 225 at 320. The wetting layer may include any one of CoB, NiB, CoP, and NiP. Electroplating of Sn or alloys of Sn can be performed at 322. Some alloys of Sn may include any one of 0.7Cu, Bi, Sb, and 3.5Ag. The photoresist may then be removed at 324 and the base layer metal 230 may be etched at 326.

Forming the die package interconnect 200 with the diffusion barrier layer 225 may entail using etching to pattern the base layer metal 230. The etching of the base layer metal 230 may reduce the degradation (e.g., corrosion or oxidation) of Sn bumps and polyimide.

Fig. 4 shows another exemplary implementation of the die package interconnect 400. The bump layer 415 is formed of Cu and is directly on top of the base layer metal 430. The base layer metal 430 may be Cu. The diffusion barrier layer 425 may be electroless and may be placed on top of the (Cu) bump layer 415 and below a layer of Sn or Sn alloy. The diffusion barrier layer 425 may provide advantages similar to the diffusion barrier layer 225 of interconnect 200 of Fig. 2. For example, the diffusion barrier layer 425 may prevent Cu and Sn diffusion or intermixing between the (Cu) bump layer 415 and the Sn layer 435 by preventing the diffusion of Cu and Sn through the diffusion barrier. The diffusion barrier layer 425 may prevent whisker formation in the bump layer 415. Although exemplary thicknesses of several layers 415, 425, 435 are shown in the diagram, layer thicknesses can vary from what is shown.

A solder layer 410 may be formed above the Sn layer 435 and a package layer 420 may be connected to the solder layer 410. The package layer 420 is electrically connected to all of the other conductive layers 410, 435, 425, 415, 430 in the interconnect 400, allowing current to flow between the die package and devices and interconnects near or on the substrate.

Fig. 5 shows an exemplary flow diagram of the fabrication of the exemplary implementation shown in Fig. 4. The process flow for interconnect 400 at 310, 312, 314, and 316 may occur in similar manners and orders as the process flow for interconnect 200 in Figs. 2-3. At 518, a Cu bump layer 415 is formed and electroplated. Electroplating the Cu bump layer 415 may provide the uniform thickness, whisker formation suppression, and low to zero compressive stress advantages as electroplating the Sn bump layer 215 in Fig. 2. The diffusion barrier layer 425 may be electroless and may be formed on the bump layer 415 at 520 and a wetting layer (not shown in Fig. 4) is formed on top of the bump layer 415 at 522. The electroless diffusion barrier layer 425 may include any one of CoBP, CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, NiWBP, and the wetting layer may include any one of CoB, NiB, CoP, and NiP.

At 524, the Sn layer 435 is formed and electroplated on top of the wetting layer. Electroplating the Sn layer 435 may provide similar advantages as described above for electroplating Sn in interconnect 200. Such similar advantages may include suppression of whisker formation and preventing low temperature phase transition of Sn. The photoresist may be removed at 516 and the base layer metal 430 may be etched at 528. A solder layer 410 may be formed above the Sn layer 435 and a package layer 420 may be connected to the solder layer 410. The solder layer 410 may contain Sn and may also be electroplated.

Fig. 6 shows another exemplary implementation of the die package interconnect 600. The bump layer 615 may be formed of Cu and may be directly on top of the base layer metal 630. The base layer metal 630 may be Cu. The diffusion barrier layer 625 may be electroless and may be placed on top of a Cu bump layer 615 and below a layer of Sn or Sn alloy. The diffusion barrier layer 625 may surround the bump layer 615, with the base layer metal 630 contacting a bottom surface of the bump layer 615. All non-base layer metal 630 surfaces of the bump layer 615, including the top surface and sidewall surfaces, may be covered with the electroless diffusion barrier layer 625. Hence, the outer surface of the bump layer 615 may be physically isolated from direct physical contact with a layer that may include Sn. The electroless

diffusion barrier layer 625 may provide advantages similar to those of interconnect 400 of Fig. 4. For example, the electroless diffusion barrier layer 625 may prevent Cu and Sn diffusion or intermixing between Cu in the bump layer 615 and Sn in a Sn layer 610, and may prevent whisker formation in the bump layer 615.

5 A solder layer 610 may be formed above the electroless diffusion barrier layer 625 and a package layer 620 may be connected to the solder layer 610. The solder layer 610 may include Sn and may be electroplated.

Fig. 7 shows an exemplary flow diagram of the fabrication of the exemplary implementation shown in Fig. 6. The processing flow for interconnect 600 at 310, 312, 314, 316
10 and 518 may occur in similar manners and orders as the processing flow for interconnect 400 in Figs. 4-5. At 720, the photoresist may be removed and the base layer metal 630 may be etched at 722. The diffusion barrier layer 625 may be electroless and may be formed on the bump layer 615 at 724 and a wetting layer (not shown in Fig. 6) may be formed on top of the bump layer 615 at 726. The electroless diffusion barrier layer 625 may include any one of CoBP, CoWP, CoWB,
15 CoWBP, NiBP, NiWP, NiWB, NiWBP, and the wetting layer may include any one of CoB, NiB, CoP, and NiP. Other conductive layers, such as the solder layer 610, may be formed on top of the electroless diffusion barrier layer 625 and the wetting layer, and can be contacted to a package layer 620.

Fig. 8 shows an exemplary implementation of the die package structure in an electrical
20 computer system. One or more interconnects and layers for a die package are formed on a substrate, as described above with respect to Figs. 3, 5, and 7. When placed on a circuit board 850, the die package 810 can connect the internal circuitry within the die package with circuitry that is external to the die package and on the circuit board 850. The circuit board 850 may have other chips and components, such as a memory 843, a central processing unit (CPU) 825, and a
25 controller or some other logic unit 833. The circuit board 850 may be made with multiple layers for routing signals between components, and may be used in a system of computers and/or electronics 860.

A number of implementations of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and
30 scope of the invention. For example, the processing order may vary from the processing order shown in Figs 3, 5, and 7. In Fig. 7, for instance, after the Cu layer has been formed and

electroplated 518 for interconnect 600, the electroless diffusion barrier layer 625 may be deposited 724. Following the formation 726 of the wetting layer on the electroless diffusion barrier layer 625, the photoresist may be removed 720 and the base layer metal 630 may be etched 722. In another example, an electroless barrier can be used to prevent the intermixing of other metals besides Cu and Sn, such as preventing the intermixing of Au and Al.

5